REMARKS

Claims 1-4, 14-15 and 18 are pending. Claims 5-13, 16 and 17 have been cancelled. The Examiner's reconsideration of the rejections is respectfully requested in view of the amendments and remarks.

The Abstract of the Disclosure has been objected to for informalities. The Abstract of the Disclosure has been amended to correct the informalities; its length is less than 150 words, and the term "comprises" has been deleted. Reconsideration of the rejection is respectfully requested.

The Drawings have been objected to; the Examiner indicated that Figure 1-3 should be designated as --Prior Art--. Corrected drawings are attached hereto. The Examiner's reconsideration of the objection is requested.

Claim 1 has been objected to in view of a potential antecedent basis problem. Claim 1 has been amended to delete the word "predetermined." Reconsideration of the rejection is respectfully requested.

Claims 1-2 and 14-15 have been rejected under 35 U.S.C. 102(e) as being anticipated by Iwamoto (USPN 6,489,823). The Examiner stated essentially that Iwamoto teaches all the limitations of claims 1-2 and 14-15.

Claim 1 claims, *inter alia*, "a delay line, comprising a plurality of delay cells having various unit time delays, for receiving the external clock signal, controlling the phase of the external clock signal to obtain an output clock signal and outputting the output clock signal, wherein the number of delay cells in operation is adjusted in response to a shift signal." Claim 14 claims, "a delay unit, comprising a plurality of delay

cells having various unit time delays, for receiving the external clock signal and generating the output clock signal in synchronization with the external clock signal."

Iwamoto teaches a delay-locked loop having a fine adjustment delay line and a course adjustment delay line (see col. 14, lines 1-9). Iwamoto does not teach "a delay line, comprising a plurality of delay cells having various unit time delays" as claimed in claims 1 and 14. The delay lines of Iwamoto include NAND circuits each corresponding to one stage serving as a minimal unit for delay adjustment (see col. 7, lines 23-26). Iwamoto's minimal unit for delay is not varied. Iwamoto does not teach a delay line including a plurality of delay cells having various unit time delays, essentially as claimed in claims 1 and 14. Indeed as noted on page 6 of the Office Action, "Iwamoto does not explicitly disclose the plurality of delay cells in the delay line 2, having various unit time delays as called for in the claim." Therefore, Iwamoto fails to teach all the limitations of claim 1 and 14.

Claims 2 and 15 depend from claims 1 and 14, respectively. The dependent claims are believed to be allowable for at least the reasons given for claims 1 and 14. The Examiner's reconsideration of the rejection is respectfully requested.

Claims 1-4 and 14-15 have been rejected under 35 U.S.C. 103(a) as being anticipated by Iwamoto in view of McCune (USPN 5,306,971). The Examiner stated essentially that the combined teachings of Iwamoto and McCune teach or suggest all the limitations of claims 1-4 and 14-15.

Claim 1 claims, *inter alia*, "a delay line, comprising a plurality of delay cells having various unit time delays, for receiving the external clock signal, controlling the phase of the external clock signal to obtain an output clock signal and outputting the

output clock signal, wherein the number of delay cells in operation is adjusted in response to a shift signal, wherein each delay cell is a differential amplifier having a resistor connected to a power supply voltage, wherein the resistor of each delay cell has a different resistance, to vary the unit time delay." Claim 14 claims, *inter alia*, "a delay unit, comprising a plurality of delay cells having various unit time delays, for receiving the external clock signal and generating the output clock signal in synchronization with the external clock signal, wherein each delay cell is a differential amplifier having a resistor connected to a power supply voltage, wherein the resistor of each delay cell has a different resistance, to vary the unit time delay."

Iwamoto teaches a delay-locked loop having a fine adjustment delay line and a course adjustment delay line (see col. 14, lines 1-9). Iwamoto does not teach or suggest a delay unit "comprising a plurality of delay cells having various unit time delays..." "wherein each delay cell is a differential amplifier having a resistor connected to a power supply voltage, wherein the resistor of each delay cell has a different resistance" essentially as claimed in claim 1 and 14. The delay lines of Iwamoto include NAND circuits each corresponding to one stage serving as a minimal unit for delay adjustment (see col. 7, lines 23-26). Iwamoto's minimal unit for delay is not varied among the NAND circuits. Thus, the additional delay of each stage of Iwamoto is equal. Iwamoto does not teach or suggest a delay unit including a plurality of delay cells having various unit time delays, much less resistors of a plurality of delay cells having different resistances, essentially as claimed in claims 1 and 14. Therefore, Iwamoto fails to teach all the limitations of claim 1 and 14.

McCune teaches a delay line comprising gates arranged from a least delay to a greatest delay (see col. 3, lines 6-11). McCune does not teach or suggest a delay unit "comprising a plurality of delay cells having various unit time delays..." "wherein each delay cell is a differential amplifier having a resistor connected to a power supply voltage, wherein the resistor of each delay cell has a different resistance" essentially as claimed in claim 1 and 14. McCune teaches that the delay of a gate is controlled by a number of transistors (see col.. 5, lines 20-41). McCune does not teach or suggest resistors of each delay cell having different resistances, essentially as claimed in claims 1 and 14. Therefore, McCune fails to cure the deficiencies of Iwamoto.

The combined teachings of Iwamoto and McCune teach a delay line comprising gates arranged from a least delay to a greatest delay. The combined teachings of Iwamoto and McCune fail to teach or suggest a delay unit "comprising a plurality of delay cells having various unit time delays..." "wherein each delay cell is a differential amplifier having a resistor connected to a power supply voltage, wherein the resistor of each delay cell has a different resistance" essentially as claimed in claim 1 and 14 (Emphasis added). Therefore, claims 1 and 14 are believed to be allowable over the combined teachings of Iwamoto and McCune.

Claims 2-4 and 15 depend from claims 1 and 14, respectively. The dependent claims are believed to be allowable for at least the reasons given for claims 1 and 14. At least claim 4 is believed to be allowable for additional reasons.

Claim 4 claims "wherein the resistance is gradually increased from the delay cell of a front end of the delay line to the delay cell of a rear end of the delay line."

Iwamoto teaches a delay-locked loop having delay lines having NAND circuits for delaying a signal (see col. 7, lines 17-30). Iwamoto does not teach or suggest "wherein the resistance is gradually increased from the delay cell of a front end of the delay line to the delay cell of a rear end of the delay line" as claimed in claim 4. Each NAND circuit of Iwamoto corresponds to a minimal unit for delay adjustment. Iwamoto fails to teach or suggest NAND circuits having different amounts of adjustment, much less, "wherein the resistance is gradually increased from the delay cell of a front end of the delay line to the delay cell of a rear end of the delay line" as claimed in claim 4. Therefore, Iwamoto fails to teach or suggest all the limitations of claim 4.

McCune teaches a delay line comprising gates arranged from a least delay to a greatest delay (see col. 3, lines 6-11). McCune does not teach or suggest "wherein the resistance is gradually increased from the delay cell of a front end of the delay line to the delay cell of a rear end of the delay line" as claimed in claim 4. McCune teaches controlling a delay according to a number of transistors (see col. 5, lines 20-41). McCune does not teach or suggest controlling a delay according to a resistor, much less, "wherein the resistance is gradually increased from the delay cell of a front end of the delay line to the delay cell of a rear end of the delay line" as claimed in claim 4. Accordingly, McCune fails to cure the deficiencies of Iwamoto.

The combined teachings or Iwamoto and McCune fail to teach or suggest "wherein the resistance is gradually increased from the delay cell of a front end of the delay line to the delay cell of a rear end of the delay line" as claimed in claim 4.

The Examiner's reconsideration of the rejection is respectfully requested.

Claim 18 includes similar limitations as that of claim 4. Claim 18 is believed to be allowable for at least the reasons given for claim 4, and for independent claim 14.

For the forgoing reasons, the application, including claims 1-4, 14-15 and 18, is believed to be in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

Respectfully submitted,

By: 

Nathaniel T. Wallace
Reg. No. 48,909
Attorney for Applicant(s)

Mailing Address:
F. CHAU & ASSOCIATES, LLC
130 Woodbury Road
Woodbury, New York 11797
TEL: (516) 692-8888
FAX: (516) 692-8889